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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,413	04/12/2004	Peter George Hartwell	10006166-4	2570

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,413	HARTWELL, PETER GEORGE	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,13,19 and 21-31* is/are rejected.

7)☒ Claim(s) *14-18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Remarks filed on 8/15/05. Currently, claims 12-31 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 10/03/05 was filed after the mailing date of the Office Action on 5/11/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12, 13, 19, 21-23, 26 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Davey US Patent 3,663,308.

Davey discloses the semiconductor method as claimed. See figures 1-11, and corresponding text, where Davey teaches, pertaining to claim 12, a method for electrically

isolating a portion of a wafer comprising: providing a first wafer **11** (figure 1a; col. 2, lines 51-55); forming a first conductor **12** at least partially through the first wafer (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position that Davey teaches that the devices are interconnected into a circuit by metallization. In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will included conductors (via structures)); disposing first dielectric material **12** between the first conductor and material of the first wafer (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will included conductors (via structures)); and at least partially surrounding the first conductor and the first dielectric material with second dielectric material **14/16**, the second dielectric material being spaced apart from the first dielectric material such that a first portion of the material of the first wafer is arranged between the first dielectric material and the second dielectric material and a second portion of the material of the first wafer is arranged outside an outer periphery of the second dielectric material (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3).

Pertaining to claim 13, Davey teaches, wherein, the first wafer has a first side and an opposing second side, and the first conductor extends through the first wafer from the first side to the second side, and further comprising: forming a second conductor **13** through the first wafer from the first side to the second side, the second conductor being arranged between the first dielectric material and the second dielectric material **15** (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3).

Pertaining to claim 19, Davey teaches, a method for electrically isolating a portion of a wafer comprising: providing a first wafer **11** having a first side and an opposing second side (figure 1a; col. 2, lines 51-53); forming a first conductor **12** through the first wafer from the first side to the second side (figures 1a and 1b; col. 2, lines 51-57)); forming a first conductor insulating layer through the first wafer, the first conductor insulating layer engaging the first conductor and being located between the first conductor and material of the first wafer, the first conductor insulating layer being formed of dielectric material (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position that Davey teaches that the devices are interconnected into a circuit by metallization. In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will included conductors (via structures)); and forming a first outer insulating layer **14/16** through the first wafer from the first side to the second side and spaced from the first conductor insulating layer such that the first outer insulating layer at least partially electrically isolates the first conductor from portions of the first wafer located outside the first insulating layer, the first outer insulating layer being formed of dielectric material (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3).

Pertaining to claim 21, Davey teaches, further comprising: forming a second conductor **13**, the second conductor extending at least partially through the first wafer, the second conductor being arranged within an area at least partially bounded by the first outer insulating layer (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3).

Pertaining to claim 22, Davey teaches, propagating a power signal via the first conductor (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position

that Davey teaches that the devices are interconnected into a circuit by metallization. In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will include conductors (via structures)).

Pertaining to claim 23, Davey teaches, propagating a data signal via the first conductor (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position that Davey teaches that the devices are interconnected into a circuit by metallization. In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will include conductors (via structures)).

Pertaining to claim 26, Davey teaches, a method for electrically isolating a portion of a wafer comprising: providing a first semiconductor wafer **11** having a substrate material (figure 1a; col. 2, lines 51-55); and forming a via structure adapted to provide electrical communication through the first wafer, the via comprising: first and second conductors **12/13** having insulating layers to form barrier with the substrate (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position that Davey teaches that the devices are interconnected into a circuit by metallization. In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will included conductors (via structures)); and an outer insulating layer **14/15/16** formed about both the first and second conductors to electrically isolate the first and second conductors from the substrate material (figure 1d; col. 2, lines 67-75; col. 3, lines 1-3).

Pertaining to claim 31, Davey teaches, propagating signals among various locations within the first wafer using the via structure of the first wafer (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position that Davey teaches that the devices

are interconnected into a circuit by metallization. In addition, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will included conductors (via structures)); disposing first dielectric material **12** between the first conductor and material of the first wafer (figures 1a and 1b; col. 1, lines 23-25; col. 2, lines 51-53, ***Note***: the Examiner takes the position, conventionally via structures include an insulating layer surrounding theses structures, as a result it is inherent that the semiconductor devices will included conductors (via structures)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24, 25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davey US Patent 3,663,308 in view of Ahn et al., US Patent 6,365, 630.

Davey discloses the semiconductor method substantially as claimed. See preceding rejection of claims 12, 13, 19, 21-23, 26, and 31 under 35 U.S.C. 102(e).

However, Davey fails to show, pertaining to claim 24, further comprising: providing a second wafer at least partially overlying the first wafer, the second wafer having a third conductor, and propagating a signal form the first conductor of the first wafer to the third conductor of the second wafer. In addition, Davey fails to show, pertaining to claim 25, wherein: the second wafer comprises: a first conductor insulating layer formed at least partially through

the second wafer, the first conductor insulating layer of the second wafer engaging the first conductor of the second wafer and being disposed between the first conductor of the second wafer and material of the second wafer, the first conductor insulating layer of the second wafer being formed of dielectric material; and a first outer insulating layer formed at least partially through the second wafer and spaced from the first conductor insulating layer of the second wafer, the first outer insulating layer of the second wafer being formed on dielectric material. Also, Davey fails to show, pertaining to claim 27, further comprising: providing a second semiconductor wafer; and locating the second semiconductor wafer; and locating the second semiconductor wafer such that the via structure provides electrical communication between the first semiconductor wafer and the second semiconductor wafer. Davey fails to show, pertaining to claim 28, wherein: the second semiconductor wafer comprises: a via structure adapted to provide electrical communication through the second wafer, the via structure comprising: first and second conductors having insulating layers the form a barrier with the substrate; and a first outer insulating layer formed about both the first and second conductors to electrically isolates the first and second conductors from the substrate material; and the method additionally comprises: arranging the second semiconductor wafer in an overlying relationship with the first wafer to form wafer stack. In addition, Davey shows, pertaining to 29, further comprising: propagating signals between the first semiconductor wafer and the second semiconductor wafer using the via structures. Finally, Davey shows, pertaining to claim 30, wherein the signals are selected from the group consisting of power signals and data signals.

Ahn teaches, in figures 1-10, and corresponding text, a similar method integrated circuit formation that includes the formation of similar via structures as taught by Forbes, where the semiconductor wafers are stacked (col. 3, lines 20-22, 30-67; col. 5, lines 1-13).

It would have been obvious to one of ordinary skill in the art to incorporate, further comprising: providing a second wafer at least partially overlying the first wafer, the second wafer having a third conductor, and propagating a signal form the first conductor of the first wafer to the third conductor of the second wafer; wherein: the second wafer comprises: a first conductor insulating layer formed at least partially through the second wafer, the first conductor insulating layer of the second wafer engaging the first conductor of the second wafer and being disposed between the first conductor of the second wafer and material of the second wafer, the first conductor insulating layer of the second wafer being formed of dielectric material; and a first outer insulating layer formed at least partially through the second wafer and spaced from the first conductor insulating layer of the second wafer, the first outer insulating layer of the second wafer being formed on dielectric material; further comprising: providing a second semiconductor wafer; and locating the second semiconductor wafer; and locating the second semiconductor wafer such that the via structure provides electrical communication between the first semiconductor wafer and the second semiconductor wafer; wherein: the second semiconductor wafer comprises: a via structure adapted to provide electrical communication through the second wafer, the via structure comprising: first and second conductors having insulating layers the form a barrier with the substrate; and a first outer insulating layer formed about both the first and second conductors to electrically isolates the first and second conductors from the substrate material; and the method additionally comprises: arranging the second semiconductor wafer in

an overlying relationship with the first wafer to form wafer stack; further comprising: propagating signals between the first semiconductor wafer and the second semiconductor wafer using the via structures; wherein the signals are selected from the group consisting of power signals and data signals., in the method of Davey, pertaining to claims 24, 25 and 27-30, according to the teachings of Ahn, with the motivation that, the via structures taught by Ahn, allow a number of semiconductor wafers to be interconnected in a stacked formation, where the advantage would be to create for example a system module the includes a greater amount of integrated circuits while having a much smaller thickness or size.

Allowable Subject Matter

Claims 14-18 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record, Davey US Patent 3,663,308 in view of Ahn et al., US Patent 6,395,630 alone or in combination, fails to show the following steps:

Pertaining to claim 14, "at least surrounding the second dielectric material with third dielectric material, the third dielectric material being spaced from the second dielectric material."

Pertaining to claim 20, "forming a second outer insulating layer through the first wafer from the first side to the second side and spaced from the first outer insulating layer such that the first outer insulating layer is arranged between the second outer insulating layer and the first conductor insulating layer, the second outer insulating layer being formed of dielectric material."

Response to Arguments

Applicant's arguments, see Remarks, filed 8/15/05, with respect to the rejection(s) of claim(s) 21-31 under 102(e) and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Davey US Patent 3,663,308 under U.S.C. 102(b) and Davey US Patent 3,663,308 in view of Ahn et al., US Patent 6,395,630 under U.S.C. 103(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
October 20, 2005

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